Claims

1. A composite amplifier circuit configured for use within high-speed applications, said composite amplifier circuit comprising:

a first amplifier having an inverting input terminal configured as an inverting input terminal for said composite amplifier circuit, and an output terminal configured as an output terminal for said composite amplifier circuit;

a second amplifier configured as an integrator circuit, said second amplifier having a non-inverting input terminal configured as a non-inverting input terminal for said composite amplifier circuit, an inverting input terminal coupled through an integrator resistor to said inverting input terminal of said composite amplifier circuit, and an output terminal coupled to a non-inverting input terminal of said first amplifier; and

a compensation circuit coupled between said output terminal of said composite amplifier circuit and said inverting input terminal of said second amplifier, said compensation circuit configured to provide a path for current needed by said integrator resistor due to any small signal appearing at said inverting input terminal for said composite amplifier circuit.

2. The composite amplifier circuit according to claim 1, wherein said compensation circuit comprises a compensation capacitor coupled between said output terminal of said composite amplifier circuit and said inverting input terminal of said second amplifier.

3. The composite amplifier circuit according to claim 2, wherein a value of said compensation capacitor is based upon a gain bandwidth product and a value of said integrator resistor.

4. The composite amplifier circuit according to claim 3, wherein said compensation capacitor comprises a single capacitor having a capacitance value between approximately 10 ff and 16 ff.

5. The composite amplifier circuit according to claim 1, wherein said integrator circuit comprises:

said integrator resistor coupled between said inverting input terminal for said composite amplifier circuit and said inverting input terminal for said second amplifier, said integrator resistor further coupled to said compensation circuit; and

a integrator capacitor coupled between said inverting input terminal for said second amplifier and said output terminal for said second amplifier.

6. The composite amplifier circuit according to claim 5, wherein said compensation circuit comprises a compensation capacitor coupled to said output terminal of said composite amplifier circuit and said integrator resistor.

7. The composite amplifier circuit according to claim 5, wherein said integrator resistor comprises at least two resistors connected together, said compensation capacitor coupled to said output terminal of said composite amplifier circuit and between said two resistors, such that a value of capacitance for said compensation can be increased

8. The composite amplifier circuit according to claim 1, wherein said first amplifier comprises a high-speed amplifier, and said second amplifier comprises a low-speed amplifier configured for correction of DC characteristics in said high-speed amplifier.

9. A method for providing a reduced settling time in an amplifier circuit, said method comprising the steps of:

generating an output signal from an output terminal of a first amplifier configured with a second amplifier comprising an integrator circuit; and

providing a compensation path between said output terminal of said first amplifier and an inverting input terminal of said second amplifier to provide any current required through an integrator resistor due to any small signal that can appear at an inverting input terminal of said amplifier circuit.

10. The method according to claim 9, wherein said step of providing a compensation path comprises providing a compensation capacitor between said output terminal of said first amplifier and said inverting input terminal of said second amplifier.

11. The method according to claim 10, wherein said step of providing a compensation capacitor comprises selecting a capacitance value based on a gain bandwidth product and a value of said integrator resistor.

12. The method according to claim 10, wherein said integrator resistor comprises at least two resistors connected together with said compensation capacitor connected in between, and wherein said step of providing a compensation capacitor comprises selecting an increased capacitance value as a result of a resistor divider network provided from said at least two resistors.

13. An amplifier circuit configured for use within high-speed applications, said amplifier circuit comprising:

a high-speed amplifier having an inverting input terminal and an output terminal;

a low-speed amplifier configured as an integrator, said low-speed amplifier having a non-inverting input terminal, an inverting input terminal coupled through an integrator resistor to said inverting input terminal of said high-speed amplifier, and

an output terminal coupled to a non-inverting input terminal of said high-speed amplifier; and

a compensation circuit coupled between said output terminal of said high-speed amplifier and said integrator resistor, said compensation circuit configured to provide a path for current needed by said integrator resistor due to any signal appearing at said inverting input terminal for said high-speed amplifier.

14. The amplifier circuit according to claim 13, wherein said compensation circuit comprises a compensation capacitor coupled between said output terminal of said high-speed amplifier and said inverting input terminal of said low-speed amplifier.

15. The amplifier circuit according to claim 14, wherein a value of said compensation capacitor is calculated based on a gain bandwidth product for said high-speed amplifier and a resistance value for said integrator resistor.

16. The amplifier circuit according to claim 13, wherein said low-speed amplifier comprises an auto-zero amplifier.

17. The amplifier circuit according to claim 14, wherein said integrator resistor comprises at least two resistors connected together with said compensation capacitor coupled to said inverting input terminal of said second amplifier through at least one of said at least two resistors.

18. The amplifier circuit according to claim 15, wherein said compensation capacitor comprises a capacitance value between approximately 10 ff and 20 ff.